Statement of Volatility – Dell PowerEdge T630

The Dell PowerEdge T630 contain both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge T630 servers.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
Planer				
PCH Internal CMOS RAM	Non-Volatile	1	U_PCH	256 Bytes
BIOS Password	Non-Volatile	1	U_PCH	16 bytes
BIOS SPI Flash	Non-Volatile	1	U_SPI_BIOS1	8 MB
iDRAC SPI Flash	Non-Volatile	1	U_IDRAC_SPI1	4 MB
BMC EMMC	Non-Volatile	1	U_EMMC1	4 GB
CPU Vcore Regulators	Non-Volatile	2	PAU1, PDU1	512 Bytes
Vmem Regulators	Non-Volatile	2	PBU1, PCU1, PEU1, PFU1	512 Bytes
System CPLD RAM	Volatile	1	U_CPLD1	1 KB
System Memory	Volatile	Up to 12 per CPU	DIMM1 ~ DIMM24	Up to 32GB per DIMM
Internal USB Key	Non-Volatile	Up to 1	N/A	Varies (not factory installed)
Trusted Platform Module (TPM)	Non-Volatile	1	U_TPM1	128 Bytes
CPU	Volatile	1 or 2	CPU1 / CPU2	Various

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Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
iDRAC DDR	Volatile	1	U_IDRAC_MEM1	256MByte
iDRAC	Volatile	1	U_IDRAC1	64 kbyte + registers
LOM EEPROM	Non-Volatile	1	U1	8Mb
LOM FLASH	Non-Volatile	1	U3	512Kb
16x2.5" EXP/Backplane (Upstream)				
NVSRAM memory	Non-Volatile	1	U_EXP_NVSRAM	1 Mb
Flash memory	Non-Volatile	1	U_EXP_FLASH	32 Mb
Expander FRU image	Non-Volatile	1	U_EXP_FRU	512 Bytes
BP FRU image	Non-Volatile	1	U_BP_FRU	256 Bytes
16x2.5" EXP/Backplane (Downstream)				
NVSRAM memory	Non-Volatile	1	U_EXP_NVSRAM	1 Mb
Flash memory	Non-Volatile	1	U_EXP_FLASH	32 Mb
Expander FRU image	Non-Volatile	1	U_EXP_FRU	512 Bytes
BP FRU image	Non-Volatile	1	U_BP_FRU	256 Bytes
8x3.5" Backplane				
SEP internal flash	Non-Volatile	1	U_SEP	Flash:32KB+4KB EEPROM: 1KB
18x3.5" Exp/Backplane				
NVSRAM memory	Non-Volatile	1	U_EXP_NVSRAM	1 Mb
Flash memory	Non-Volatile	1	U_EXP_FLASH	32 Mb
BP FRU image	Non-Volatile	1	U_EXP_FRU	256 Bytes
Expander FRU image	Non-Volatile	1	U_BP_FRU	512 Bytes
4x PCIe SSD Backplane				
SEP internal flash	Non-Volatile	1	U_SEP	Flash:32KB+4KB EEPROM: 1KB
H730, H830 PERCs				
NVSRAM	Non-volatile	1	U1033	128KB
FRU	Non-volatile	1	U1019	256B
1-Wire EEPROM	Non-volatile	1	U1004	128B
SPD	Non-volatile	1	U22	256B

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Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
SBR	Non-volatile	1	U1020	8KB
Flash	Non-volatile	1	U1031	16MB
ONFI Backup Flash	Non-volatile	1	U1059	4GB
SDRAM	Volatile	5	U1043-U1047	512MB/1GB
H330 PERC				
NVSRAM	Non-volatile	1	U1033	128KB
FRU	Non-volatile	1	U1019	256B
1-Wire EEPROM	Non-volatile	1	U1004	128B
SBR	Non-volatile	1	U1020	8KB
Flash	Non-volatile	1	U3	16MB
PCIe SSD Extension Card				
Switch Configuration EEPROM	Non-Volatile	1	U2	256B
IDSDM				
SPI Flash	Non-Volatile	1	U2	8Mb
MCU	Non-Volatile	1	U6	512KB
Front Panel				
SPI Flash	Non-Volatile	1	U_SPI_FLASH	32Mb

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Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?
Planer		
PCH Internal CMOS RAM	Battery-backed CMOS RAM	No
BIOS Password	Battery-backed CMOS RAM	Yes
BIOS SPI Flash	SPI Flash	No
iDRAC SPI Flash	SPI Flash	No
BMC EMMC	eMMC NAND Flash	No
CPU Vcore Regulators	ROM	No
Vmem Regulators	ROM	No
System CPLD RAM	RAM	No
System Memory	DRAM	Yes
Internal USB Key	Flash	Yes
Trusted Platform Module (TPM)	EEPROM	Yes
CPU	Cache + registers	Yes
iDRAC DDR	DRAM	No
iDRAC	Cache + registers	No
LOM EEPROM	EEPROM	Yes
LOM FLASH	Flash	Yes
16x2.5" EXP/Backplane (Upstream)		
NVSRAM memory	Flash	No

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Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?
Flash memory	Flash	No
Expander FRU image	I2C EEPROM	No
BP FRU image	I2C EEPROM	No
16x2.5" EXP/Backplane (Downstream)		
NVSRAM memory	Flash	No
Flash memory	Flash	No
Expander FRU image	I2C EEPROM	No
BP FRU image	I2C EEPROM	No
8x3.5" Backplane		
SEP internal flash	Integrated Flash+EEPROM	No
18x3.5" Exp/Backplane		
NVSRAM memory	Flash	No
Flash memory	Flash	No
BP FRU image	I2C EEPROM	No
Expander FRU image	I2C EEPROM	No
4x PCIe SSD Backplane		
SEP internal flash	Integrated Flash+EEPROM	No
H730, H830 PERCs		
NVSRAM	NVSRAM	No
FRU	FRU	No
1-Wire EEPROM	1-Wire EEPROM	No
SPD	SPD	No
SBR	SBR	No
Flash	Flash	No
ONFI Backup Flash	ONFI Backup Flash	No
SDRAM	SDRAM	No
H330 PERC		
NVSRAM	NVSRAM	No
FRU	FRU	No
1-Wire EEPROM	1-Wire EEPROM	No

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Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?
SBR	SBR	No
Flash	Flash	No
PCIe SSD Extension Card		
Switch Configuration EEPROM	SPI Flash EEPROM	No (requires specialized SW)
IDSDM		
SPI Flash	SPI Flash	No
MCU	Embedded Flash	FW can be updated via iDRAC which runs on Linux
Front Panel		
SPI Flash	SPI Flash	No

Item	Purpose? (e.g. boot code)	How is data input to this memory?
Planer		
PCH Internal CMOS RAM	Real-time clock and BIOS configuration settings	BIOS
BIOS Password	Password to change BIOS settings	Keyboard
BIOS SPI Flash	Boot code, system configuration information, UEFI environment, Flash descriptor, ME	SPI interface via iDRAC
iDRAC SPI Flash	iDRAC Uboot (bootloader), server management persistent store (i.e. IDRAC MAC Address, iDRAC boot variables), lifecycle log cache, virtual planar FRU and EPPID, rac log, system event log, JobStore, iDRAC Secure boot code,	SPI interface via iDRAC

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Item	Purpose? (e.g. boot code)	How is data input to this memory?
BMC EMMC	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware	NAND Flash interface via iDRAC
CPU Vcore Regulators	Operational parameters	
Vmem Regulators	Operational parameters	
System CPLD RAM	Not utilized	Not utilized
System Memory	System OS RAM	System OS
Internal USB Key	General purpose USB key drive	USB interface via PCH. Accessed via system OS
Trusted Platform Module (TPM)	Storage of encryption keys	Using TPM Enabled operating systems
CPU	Processor cache + registers	Various
iDRAC DDR	iDRAC local memory	iDRAC Firmware
iDRAC	Processor cache + registers	iDRAC Firmware
LOM EEPROM	Onboard LOM FW	
LOM FLASH	Onboard LOM FW	
16x2.5" EXP/Backplane (Upstream)		
NVSRAM memory	FW config data	Common Flash memory Interface (CFI)
Flash memory	Firmware	Common Flash memory Interface (CFI)
Expander FRU image	FRU	I2C interface via iDRAC
BP FRU image	FRU	I2C interface via iDRAC
16x2.5" EXP/Backplane (Downstream)		
NVSRAM memory	FW config data	Common Flash memory Interface (CFI)
Flash memory	Firmware	Common Flash memory Interface (CFI)
Expander FRU image	FRU	I2C interface via iDRAC
BP FRU image	FRU	I2C interface via iDRAC
8x3.5" Backplane		
SEP internal flash	Firmware + FRU	I2C interface via iDRAC
18x3.5" Exp/Backplane		
NVSRAM memory	FW config data	Common Flash memory Interface (CFI)
Flash memory	Firmware	Common Flash memory Interface (CFI)
BP FRU image	FRU	I2C interface via iDRAC
Expander FRU image	FRU	I2C interface via iDRAC
4x PCIe SSD Backplane		
SEP internal flash	Firmware + FRU	I2C interface via iDRAC
H730, H830 PERCs		
NVSRAM	Configuration data	ROC writes configuration data to NVSRAM

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Item	Purpose? (e.g. boot code)	How is data input to this memory?
FRU	Card manufacturing information	Programmed at ICT during production.
1-Wire EEPROM	Holds default controller properties/settings	ROC writes data to this memory
SPD	Memory configuration data	Pre-programmed before assembly
SBR	Bootloader	Pre-programmed before assembly
Flash	Card firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools
ONFI Backup Flash	Holds cache data during power loss	FPGA backs up DDR data to this device in case of a power failure
SDRAM	Cache for HDD I/O	ROC writes to this memory - using it as cache for data IO to HDDs
H330 PERC		
NVSRAM	Configuration data	ROC writes configuration data to NVSRAM
FRU	Card manufacturing information	Programmed at ICT during production
1-Wire EEPROM	Holds default controller properties/settings	ROC writes data to this memory
SBR	Bootloader	Pre-programmed before assembly
Flash	Card firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools
PCIe SSD Extension Card		
Switch Configuration EEPROM	Configuration for PLX PCIe switch, setting registers	The EEPROM image is pre-loaded at factory before assembly. Once assembled on the card, data can be entered via PLX Device Editor or PLX EEP DOS based tool.
IDSDM		
SPI Flash	Exclusively used by the controller	SPI interface via iDRAC
MCU	Firmware	USB3.0 interface via PCH
Front Panel		
SPI Flash	For field maintenance. Have License, Service Tag and system information.	SPI interface via iDRAC

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Item	How is this memory write protected?	How is the memory cleared?
Planer		
PCH Internal CMOS RAM	N/A – BIOS only control	1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system; 2) AC power off system, remove coin cell battery for 30 seconds, replace battery and power back on; 3) restore default configuration in F2 system setup menu.
BIOS Password	N/A	Place shunt on J_PSWD_NVRAM jumper pins 2 and 4.
BIOS SPI Flash	Software write protected	Not possible with any utilities or applications and system is not functional if corrupted/removed.
iDRAC SPI Flash	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface
BMC EMMC	Embedded FW write protected	Not completely user clearable; however, user data, lifecycle log and archive, SEL, fw image repository can be cleared via Delete Configuration and Retire System, accessible in Lifecycle Controller interface
CPU Vcore Regulators	NA	Not user clearable
Vmem Regulators	NA	Not user clearable
System CPLD RAM	Not accessible	Not accessible
System Memory	OS Control	Reboot or power down system
Internal USB Key	No write protect	Can be cleared in system OS
Trusted Platform Module (TPM)	SW write protected	F2 Setup option
CPU	Various	Power off
iDRAC DDR	NA	Power off
iDRAC	NA	Power off
LOM EEPROM	NA	Not user clearable
LOM FLASH	NA	Not user clearable

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Item	How is this memory write protected?	How is the memory cleared?
16x2.5" EXP/Backplane (Upstream)		
NVSRAM memory	Hardware strapping	Not user clearable
Flash memory	Hardware strapping	Not user clearable
Expander FRU image	Hardware strapping	Not user clearable
BP FRU image	Hardware strapping	Not user clearable
16x2.5" EXP/Backplane (Downstream)		
NVSRAM memory	Hardware strapping	Not user clearable
Flash memory	Hardware strapping	Not user clearable
Expander FRU image	Hardware strapping	Not user clearable
BP FRU image	Hardware strapping	Not user clearable
8x3.5" Backplane		
SEP internal flash	Program write protect bit	Not user clearable
18x3.5" Exp/Backplane		
NVSRAM memory	Hardware strapping	Not user clearable
Flash memory	Hardware strapping	Not user clearable
BP FRU image	Hardware strapping	Not user clearable
Expander FRU image	Hardware strapping	Not user clearable
4x PCIe SSD Backplane		
SEP internal flash	Program write protect bit	Not user clearable
H730, H830 PERCs		
NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SPD	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SBR	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
ONFI Backup Flash	Not WP. Not visible to Host Processor	Flash can be cleared by powering up the card and allowing the controller to flush the contents to VDs. If the VDs are no longer available, cache can be cleared by going into controller bios and selecting Discard Preserved Cache.

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Item	How is this memory write protected?	How is the memory cleared?
SDRAM	Not WP. Not visible to Host Processor	Cache can be cleared by powering off the card
H330 PERC		
NVSRAM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Not WP	Cannot be cleared with existing tools available to the customer
1-Wire EEPROM	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
SBR	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Flash	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
PCIe SSD Extension Card		
Switch Configuration EEPROM	Device can be write protected via hardware pin. Alternatively, device contents can be write protected via WPEN bit in status register.	System is not functional as intended if corrupted/removed.
IDSDM		
SPI Flash	Hardware strapping	Not user clearable
MCU	N/A	Not user clearable
Front Panel		
SPI Flash	Hardware strapping	Not user clearable

NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.

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